Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **OUTPUT 2**
2. **OUTPUT 1**
3. **V+**
4. **INPUT 1-**
5. **IMPUT 1+**
6. **IMPUT 2-**
7. **IMPUT 2+**
8. **IMPUT 3-**
9. **IMPUT 3+**
10. **INPUT 4-**
11. **INPUT 4+**
12. **GND**
13. **OUTPUT 4**
14. **OUTPUT 3**

**.042”**

**.041”**

**2 1 14 13**

**3**

**4**

**5**

**6 7 8 9**

**12**

**11**

**10**

**MASK**

**REF**

**1901H**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND or FLOATING**

**Mask Ref: 1901H**

**APPROVED BY: DK DIE SIZE .041” X .042” DATE: 11/2/21**

**MFG: NATIONAL THICKNESS .013” P/N: LM139MDE**

**DG 10.1.2**

#### Rev B, 7/19/02